UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,266	01/22/2002	Ki-won Choi	9898-208	6747

7590 07/09/2004

MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, OR 97205

EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,266	CHOI, KI-WON	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-16,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-16,26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1, 3-4, 6-10, 13, 16, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,468,994 to Pendse in view of US Patent No. 6.232.561 to Schmidt et al.

Regarding claim 1, Pendse (figure 4) teaches a semiconductor package comprising:

a substrate (22) including a pad (16), an pad (30) connected to a solder ball (8);

a semiconductor chip (34) having a bond pad (a bond pad is located on the chip [34]) attached to the substrate (22);

a normal wire bonding unit (38) coupled between the bond pad (a bond pad is located on the chip [34]) and the pad (16).

It is inherently for the pad (16), pad (30), bond pad (a bond pad is located on the chip [34]) and solder ball (8), which are a redundant bond finger, added bond finger, added bond pad and redundant solder ball, respectively because they provide interconnection.

Pendse differs from the claimed invention by not showing an added wire bonding unit coupled between the redundant bond finger and the added bond finger. However, Schmidt et al.

(figure 2b) teach a wire bonding unit (6) coupled between the conductor pad (4) (redundant bond finger) and the conductor pad (3) (added bond finger). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Schmidt et al. into the device taught by Pendse because it provides interconnections. The combined device shows an added wire bonding unit coupled between the redundant bond finger and the added bond finger, wherein the added bond pad is electrically connected to the redundant solder ball via the redundant bond finger and the added bond finger.

Regarding claim 3, the combined device inherently teaches a solder ball connected to the redundant solder ball pad.

Regarding claim 4, the combined device teaches the substrate (Pendse; 22) is a single layer substrate. It is inherent to have printed circuit patterns because the printed circuit patterns are used to connect the chip and the solder balls.

Regarding claim 6, it is inherent that a solder mask is not formed on the added bond finger because Pendse never discloses a solder mask.

Regarding claim 7, the combined device shows the added wire bonding unit is formed over the substrate (Pendse; 22).

Regarding claim 8, the combined device shows the added wire bonding unit is formed on an outer region of the substrate (Pendse; 22) on which the semiconductor chip (Pendse; 34) is mounted.

Regarding claim 9, the combined device shows the added wire bonding unit is one unit.

Regarding claim 10, the combined device shows the semiconductor chip (Pendse; 34) is attached to the substrate (Pendse; 22) using an adhesive (Pendse; 36).

Regarding claim 13, Pendse (figure 4) teaches a semiconductor package comprising:

a substrate (22) including a first printed circuit pattern (a printed circuit pattern is formed between the pad [16] and the pad [30]) connect to pad (16) and a second printed circuit pattern (a printed circuit pattern is formed between the pad [30] and the solder ball [8]) connected to a solder ball (8);

a semiconductor chip (34) attached to the substrate (22).

It is inherently for the pad (16), pad (30) and solder ball (8), which are a redundant bond finger, added bond finger and redundant solder ball, respectively because they provide interconnection.

Pendse differs from the claimed invention by not showing an added wire bonding unit coupled between the redundant bond finger and the added bond finger. However, Schmidt et al. (figure 2b) teach a wire bonding unit (6) coupled between the conductor pad (4) (redundant bond finger) and the conductor pad (3) (added bond finger). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Schmidt et al. into the device taught by Pendse because it provides interconnections. The combined device shows an added wire bonding unit coupled between the first printed circuit pattern to the second printed circuit pattern to electrically connect the redundant bond finger to the redundant solder ball.

Regarding claim 16, the combined device inherently teach the first printed circuit pattern and a second printed circuit pattern each have a width that enables wire bonding to be performed thereon.

Regarding claim 26, Pendse (figure 4) teaches a semiconductor package comprising:

a semiconductor chip (34) having a bond pad (a bond pad is located on the chip [34]);

a substrate (22) having a pad (16) and a pad (30) connected to a solder ball (8);

a normal wire bonding unit (38) coupled between the bond pad (a bond pad is located on the chip [34]) and the pad (16).

It is inherently for the pad (16), pad (30), bond pad (a bond pad is located on the chip [34]) and solder ball (8), which are a redundant bond finger, added bond finger, added bond pad and redundant solder ball, respectively because they provide interconnection.

Pendse differs from the claimed invention by not showing an added wire bonding unit coupled between the redundant bond finger and the added bond finger. However, Schmidt et al. (figure 2b) teach a wire bonding unit (6) coupled between the conductor pad (4) (redundant bond finger) and the conductor pad (3) (added bond finger). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Schmidt et al. into the device taught by Pendse because it provides interconnections. The combined device shows an added wire bonding unit coupled between the redundant bond finger and the added bond finger such that the added bond pad is electrically connected to the redundant solder ball via the redundant bond finger and the added bond finger.

Regarding claim 27, the combined device shows the added bond finger (Pendse [30]) is not directly connected to the added bond pad (Pendse; a bond pad is located on the chip [34])

3. Claims 2, 5, 12, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pendse in view of Schmidt et al., and further in view of Applicant Admitted Prior Art (AAPA).

Regarding claim 2, the combined device differs from the claimed invention by not showing an encapsulant for encapsulating the semiconductor chip, the normal and added wire bonding units. However, AAPA (figures 1-2) teaches an encapsulant (7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate an encapsulant of AAPA into the device of Pendse and Schmidt et al. because it protects device from the external environment. The combined device shows that an encapsulant for encapsulating the semiconductor chip, the normal and added wire bonding units.

Regarding claim 5, the combined device differs from the claimed invention by not showing the substrate is a double layer substrate or a multi layer substrate. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the substrate is a double layer substrate or a multi-layer substrate because it depends on the size of the package.

Regarding claim 12, the combined device differs from the claimed invention by not showing the added bond finger has the same pad shape as that of the redundant bond finger. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the added bond finger has the same pad shape as that of the redundant bond finger because it depends on the size of the substrate.

Regarding claim 14, the combined device differs from the claimed invention by not showing an encapsulant for encapsulating the semiconductor chip and the added wire bonding units. However, AAPA (figures 1-2) teaches an encapsulant (7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate an encapsulant of AAPA into the device of Pendse and Schmidt et al. because it protects device

from the external environment. The combined device shows that an encapsulant for encapsulating the semiconductor chip and the added wire bonding units.

Regarding claim 15, the combined device inherently teaches a solder ball connected to the redundant solder ball pad (8).

Response to Arguments

Applicant's arguments with respect to claims 1-10, 12-16, 26 and 27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
July 1, 2004

Sara Crane
Primary Examiner